IV. REMARKS

1. Claim 9 is amended to correct a typographical error that does not further narrow or limit the scope of the claim. Claims 36-41 are new.

2. Claim 3 is not anticipated by Sugai under 35 U.S.C. §102(b). In this application Applicants are claiming an adjustable termination path is switchable between an open emitter pulldown and matching impedance. However, Applicants also claim that the device provides a line to line impedance of the first data bus to the second data bus. Sugai's patent is not capable of supporting a differential data bus comprised of a differential twisted pair line as claimed.

The termination scheme disclosed in Sugai is a frequency limited termination method (Capacitance 28 in Figure 3, 6, 7). This is a modification of the popular AC termination method commonly used for many years with on-board and short cable termination.

The AC termination method shown in Sugai is frequency limited based on the fact that as frequency goes up, there is a low pass filtering effect with the turnover frequency of the clock or data signals. This is based on $F_C = 1 / (SQRT (2 \times Pi \times R \times C)$. The larger the capacitor, the lower the turnover frequency, hence the lower clock and data rates that are usable. The capacitor value is calculated based on RC delay of 2 times the round trip time delay of the system cabling. Since cable velocity delays are much higher that Printed Wiring Board PWB delays, this causes the capacitor value to be high. It should be noted that Applicants' invention does not include such a capacitor for reasons described herein.

The AC termination method of Sugai has signal attenuation characteristics of $X_C = 1 / (2 \times Pi \times R \times C)$. As clock and data rates go up, the capacitor impedance (X_C) is lower. The capacitor value is calculated to cause it to appear as a low impedance for the transition edge. This makes the capacitor look like a short, applying the resistive element to terminate the line. Since the capacitor value is higher for cable termination, the system impedance is lower for the intended signals as well as the transition edge. The lower capacitor impedance attenuates the received voltage level of the intended signal at the receiver, degrading system performance at high clock and data rates.

While the AC termination method of Sugai works well for low frequency clocks with fast transition edge rates, it is not effective at higher clock rates (the higher clock rates begin to be attenuated by the turnover frequency). The AC termination method is often problematic with high rate bursted data (data that has been high or low for a long period of time, then creates a short duty cycle pulse train). The small value capacitor used for terminating the transition edge does not supply the required current from being "marked" or "spaced" for a long period of time. This often results in missing the start bit of a data stream. For this reason, it is not recommended to use AC termination of Sugai for "data" signaling. It may be used for "lower rate clock" signaling but not for "high rate clock" signaling. Applicants' invention overcomes this problem.

The AC termination method of Sugai is also limited in that it often will react with interface cable capacitance (adds to it because of the higher capacitor value used) and inductance creating cable resonant impedance nodes. These nodes cause level shifting which may cause data loss, as the system response is not

flat. While cable resonant frequencies may occur in many systems, the higher value capacitor in the AC termination method seriously degrades this condition.

Often with the AC termination method of Sugai, there is "walk-out" on the trailing transition edge. This walk-out is caused by the reverse charging of the capacitor, inductance, and the relatively high input impedance seen by the receiver. This walk-out prevents rapid charging (integration effect of the capacitor) of the line, limiting the maximum frequency capability of the system.

The AC termination method of Sugai also assumes that the driver supplies a voltage/current source for creating the clock and data signals. Some interfaces (ECL, GTL, etc) use open Emitter (or FET Source) or open Collector (or FET Drain) outputs and require a pull-down or pull-up to create the logic level at the source or destination. High rate data signaling usually requires current mode interface techniques (ECL, LVDS, GTL, etc), which requires the pull-down, or pull-up. AC termination is not usually used for high rate interfaces.

The AC termination method of Sugai uses capacitors, which introduce poor environmental performance as their manufacturing tolerances are 5% to 20% typical. The capacitor tolerance varies over temperature and age, causing the value to change. The variance in capacitance creates a variable turnover frequency and variable impedance. In high rate clock and data rate signaling environments, the termination mismatch or differential imbalance from the two capacitors is unacceptable and causes noise margin degradation in hostile environments. The termination resistor also has tolerance, but 1% tolerance or better resistors are easy

to obtain. Even if a 1% tolerance capacitor was used, it still adds to the impedance discontinuities of the system.

The termination method Applicants' invention as claimed is not frequency limited as detailed above and provides a wide bandwidth (DC to high MHz) interface.

The termination method of Applicants' invention as recited in the claims is based on a direct-coupled approach. There is no series capacitor to cause a turnover frequency to limit performance. Performance is limited by drive capability, cable loss (dB/ft) and dispersion, connector performance, noise environment, and differential receiver recovery performance.

Since the termination method recited in the claims requires no series capacitor, the termination method works well for both clock and data signaling. Unlike Sugai, the termination method of Applicants' invention responds well to high clock and data rates and bursted data signaling.

The termination method of Applicants' invention also does not create additional impedance nodes, system response is much flatter, and cable resonance problems are kept to a minimum.

The termination method recited in the claims also does not suffer from walk-out associated the AC termination method which limits data signaling system performance.

The termination method in Applicants' invention provides a logic level (via pull-down and/or pull-up resistors through the switched FET) for current mode interface operation required for high clock and data rates and return current control techniques.

Also the termination method in Applicants' invention as claimed does not use a capacitor that would introduces poor environmental performance and suffers from aging and mechanical effects. The termination is more consistent over time and limited only by the FET RDS_{ON}, C_{GS}, and resistor tolerance. In high rate clock and data rate signaling environments, Applicants' device provides acceptable noise margin degradation in hostile environments. Since the termination resistor tolerance is 1% or better, system impedance discontinuities of the system are kept to a minimum.

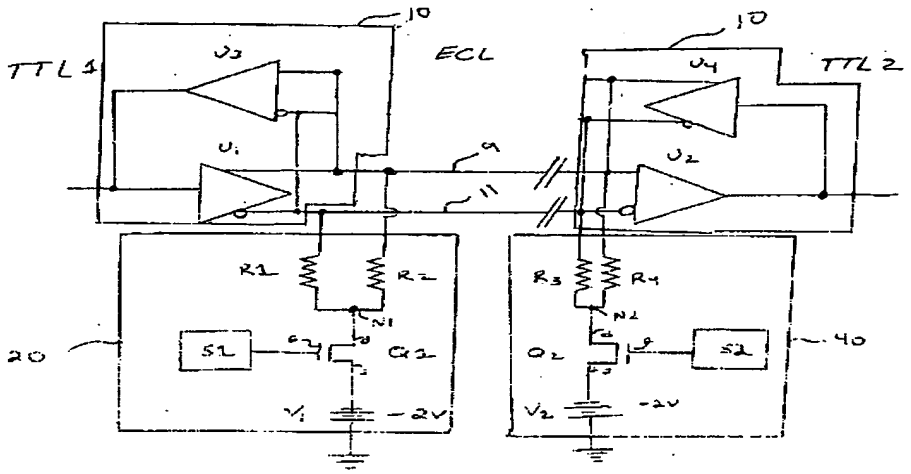
Sugai also fails to disclose or suggest that the second adjustable termination is switchable between a line to line impedance of the first data us and the second data bus as recited in claims 3, 4 and 12.

Sugai also fails to disclose or suggest that the twisted pair line 12 (12a, 12b) of FIG. 6 is switchable between - 2 volts (VTT-VD) or a short that connects the first transmission line 12a and the second transmission line 12b. Rather, in the differential signal switch circuit of Sugai illustrated in FIG. 6, when the switching element 25 is turned ON by the control signal C, current is pulled in toward the power source VTT-VD via the switching diodes 21a, 21b and 22. When the switch element 25 is turned off by the control signal C, the diode 23 is turned on and diodes 21a, 21b and 22 are turned off. (Col. 6, lines 54-62). No where in Sugai is it disclosed or suggested that a short connects the first data bus and the second data bus as suggested by the Examiner.

In Applicants' invention, referring to FIG. 3 reprinted below, the devices 20, 40 each comprise current resistors R1-R4 that are generally equivalent to the characteristic impedance of the transmission line. Each switch is connectable to a voltage supply V_1, V_2, generally - $2VD_c$. The resistors R1, R2 are connectable to the ECC differential data bus 10.

When switch Q1 is "open", resistors R1 and R2 are in series between the lines of the differential data bus. When Q1 is "closed" the lines of the data bus are terminated.

FIG. 3



Thus, there are very distinct differences between Applicants' invention as recited in the claims and the invention of Sugai. Thus, claim 3 cannot be anticipated by Sugai.

Claims 4, 12, 13, 14, 19, 24, 28 and 32 recited similar non-disclosure features and should also be allowable.

Claims 2, 5, 7, 8, 11, 15-17, 20-23, 25-27, 29-31, 34 and 35 should also be allowable at least in view of the respective dependencies.

3. Claims 5, 9, 11, 16, 18, 19-23, 25 and 29 are not unpatentable over Sugai under 35 U.S.C. §103(a).

Applicants' respectfully disagree with the Examiners conclusions regarding claim 18 and request the Examiner to provide evidence of his assertions.

Furthermore, it is submitted that the features of claims 5, 9, 12, 14, 18, 19, 24 and 28 are not disclosed or suggested by Sugai. Claims 11, 16, 20-23, 25 and 29 should be allowable at least in view of their respective dependencies.

For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record, and are in proper form for allowance. Accordingly, favorable reconsideration and allowance is respectfully requested. Should any unresolved issues remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

A check in the amount of $218 is enclosed for additional claim fees and a one-month extension of time. The Commissioner is hereby authorized to charge payment for any fees associated with this communication or credit any over payment to Deposit Account No. 16-1350.

Respectfully submitted,

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